Module Specifications

*for*

ETHIIC (ETH to I2C)

*a derivative of*

IO Extender Module

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| *Version* | *Date* | *Description* |
| 1 | Nov 17, 2010 | Basic version |
| 1.1 | Mar 1, 2011 | Serial Communication block added |
| 1.2 | Apr 15, 2012 | Added read and write byte capability on IIC bus |
| 1.3 | Jul 10, 2014 | Added wakeup sequence capability for IIC bus |

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# General

## Scope

This document provides the full list of development requirements for the VCortex ETHIIC device. It may also be a basis for any test procedures that will be developed for the device.

## Overview

VCortex color control scanner is installed on printing presses, which are complex machines with various sensors, devices that must be read for proper scanning, and others that must be controlled for color control operation.

Since the scanner includes a PC and GBE switch, the most convenient way to interface to press components is by Ethernet, where possible. Where it’s not possible, a bridge is required.

The ETHIIC (Ethernet Integrated InterCom) is such bridge. It will provide interface to various standard communication channels via Ethernet.

ETHIIC is a daughter board, which is hosted by a mother board that provides electromechanical connection to the machine, power, etc. This configuration allows cheap and simple mother board, customized for each press or specific device in the press.

The ETHIIC is a partial implementation of the IOX (IO Extender module) that includes some more interfaces implementation. The GPIO and IIC are fully implemented in the ETHIIC board, as a derivative of the IOX module.

The ETHIIC can be connected as a single or multiple configuration, controlled by host computer through UDP commands.

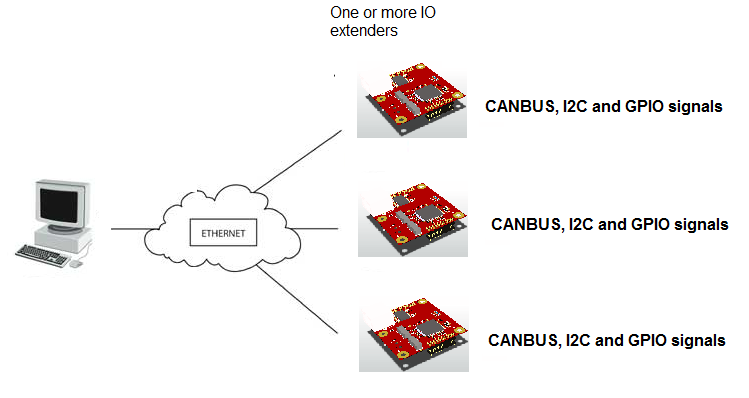


Figure : IOX multiple board configuration

# Capabilities

## Electrical Interfaces

ETHIIC interfaces are:

1. CAN

Two CAN channels are planned. CAN transceiver is not required and will be added on mother board for ETHIIC cost reduction. The channel specifications are:

* Up to 1Mbps programmable baud rate
* Protocol:2.0, 11 bits address/identifier
* Broadcast address: programmable

1. UART

Two UART channels are planned. Each channel will be initialized to certain configuration prior usage.

* Supported baud rates: 9600, 19200, 38400, 57600, 115200
* Data bits: 8 (optionally 7)
* Stop bits: 1 or 2
* Parity: None (optionally even, odd, 0, 1)

1. I2C

Two I2C channels will be available:

* Supported baud rates: 100k, 400k (optionally faster)
* Send buffer to address (up to 256 bytes)
* Read buffer from address (up to 256 bytes)

1. Analog

* At least 10 analog inputs.
* At least 4 analog outputs (IOX only)
* Separate power supply, provided from mother board (ETHIIC)
* 12 bit conversion
* 0 to 3.3V range
* No buffers, filters or other analog circuits
* Asynchronous read
* Optionally return buffer of all channels sampled one after another with minimal delay

1. GPIO

All GPIO will be selected instead other functions on same pins. For some pins pull ups may exist on board. In other case, a buffer can be provided by the supporting motherboard.

* Voltage: 3.3V
* Drive current: 4mA
* Output or input
* Read/write functions will operate separate outputs/inputs, or all of them at a time.

## IP communication

### Physical layer speed

Ethernet communication speed will be 10/100MBits/sec.

### Communication protocol

All commands to modify or read IO channels values will be implemented throu UDP/IP communication. All UDP commands will require a response from the ETHIIC module, which will determined whether the communication has arrived, and operation succeeded or failed. Each command will bare 3 retries before communication failure is declared. Timeout for retry is 1 sec.

### Addressing

Each ETHIIC board will bear a unique name and unique IP. The name will be its ID in the network. The MAC address will be derived from the IP number (fixed number that has same last number as the IP number).

Board name and IP will be modifiable through web server.

Default IP address: 10.0.0.131

Default MAC address: 00-1a-b6-02-c6-83

### Web server

The ETHIIC firmware will implement an HTTP web server to update and display board parameters, as well as some communication logs.

### Ping support

The FW will support Ping with max time of 3mSec.

### DHCP support

The board FW will support DHCP addressing (optional).

## Host driver

ETHIIC will be supported by c++ DLL (extern “c” call type). Following features will be implemented:

### Init device

Input: Board logical name

Output: Device Handle.

This function will translate the logical name to IP address, by sending a broadcast who-is message to all boards on the net. Then the IP address of the identified board will be noted for later commands. The application

### Init IIC

Input: Device Handle, IIC speed

This function will initialize the IIC device on the ETHIIC board.

### Write bytes

Input: Device Handle, slave address, buffer length

Output: buffer of bytes

This function writes the bytes in the buffer on the IIC bus, preceded by slave address.

### Read bytes

Input: Device Handle, slave address, buffer of bytes, buffer length

This function sets the slave address on the IIC bus, and then reads N bytes from the buss.

### Write and read byte

Input: Device Handle, slave address, byte to write

Output: byte read

This function writes and reads one byte

### Send wakeup sequence

Input: Device Handle, slave address

This function writes the slave address on the bus, and then follows with a series of logical settings to the IIC bus

### Close device

Input: Device handle

This function closes the device handle and releases all resources allocated to it.

## Mechanical

The board size will be as small as possible, with dimensions close to 50mm X 70mm